Hall Ticket Number:

Code No. : 41524 S

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD
B.E. (IT) IV Year I-Semester Supplementary Examinations, May-2019
VLSI Design

Time: **3** hours Max. Marks: **70**

*Note:Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Give the syntax for NMOS and PMOS Switches supported by Verilog HDL.
2. List various gate delays supported by Verilog HDL.
3. Illustrate the concept of Bubble Pushing with example.
4. What is body bias effect? And how does it affect threshold voltage?
5. Draw side-view and top-view of NMOSFET and PMOSFET.
6. List the layers used to create MOSFET.
7. List lambda based designed rules for polysilicon and n-well.
8. Define rise time and fall time in CMOS inverter and give the expression for it.
9. Draw the generalized block diagram for NOR Based ROM.
10. Why SRAM is faster switching compared to DRAM, give details.

Part-B (5 ×10=50 Marks)

11. a) Write a short note on various timing controls supported by Behavioural modeling. [5]
    b) Write a Verilog code to design 4 by 1 multiplexer in gate level modeling. [5]
12. a) Design a CMOS logic for AOI F = $\overline{AB + CD}$. [5]
    b) Design XOR and XNOR gate using transmission gate based logic. [5]
13. a) Draw the layouts for series and parallel connected FETs. [5]
    b) Draw the stick diagram for CMOS logic F = $\overline{A(B + C)}$. [5]
14. a) Write a short note on cell based design. [4]
    b) Drive the expression for minimum delay in inverter cascade. [6]
15. a) Explain the operation of 8-bit carry skip adder with neat diagram. [4]
    b) Describe read and write operation of 6T-SRAM cell with diagram. [6]
16. a) Differentiate between blocking and non-blocking assignment in verilog HDL. [4]
    b) Derive the expression for Drain current (I_{DS}) for nMOS transistor. [6]
17. Answer any ***two*** of the following:
    a) Draw the layouts of following basic structures [5]
       i) n-well
       ii) mask for nFET
       iii) mask for pFET
    b) Discuss in brief DC characteristics of CMOS inverter and derive the expression for mid-point voltage (V_M). [5]
    c) Explain read and write operation of 1-T DRAM cell with neat diagram. [5]